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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,574	06/15/2005	John M Yarborough JR.	PHUS020590	9450

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
GOODLEY, JAMES E	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 10/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/538,574	YARBOROUGH, JOHN M	
	Examiner	Art Unit	
	James E. Goodley	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *15 June 2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

JG

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Kodama (US 6,300,843 - of record)***.

Regarding **claim 1**, Fig. 3 of Kodama discloses an oscillator [200] comprising:

a first resistor [121], a second resistor [123], and a capacitor [30], wherein an oscillation frequency of the oscillator is dependent upon a difference between a first resistance value of the first resistor and a second resistance value of the second resistor, the first resistance value being larger than the second resistance value, the first resistor exhibits a first rate of change with temperature (regulation of resistance relative to temperature), and the second resistor exhibits a second rate of change with temperature that is larger than the first rate of change (see lines 12-14 of column 8), thereby allowing temperature-induced changes to the first resistance value to be offset

by changes to the second resistance value, and thereby reducing variations in the oscillation frequency with temperature (see lines 64-67 of column 1).

Regarding **claims 2-4**, Fig. 1 of Kodama discloses the oscillator of claim 1, further comprising:

a first stage [resistances 21 and 23 and NMOS 29], operably coupled to the first resistor, that is configured to provide a first voltage level [at node N3 to contribute to voltage at node N5], based on the first resistance value,

a second stage [resistances 23 and 25 and NMOS 27], operably coupled to the second resistor, that is configured to provide a second voltage level [at node N4 to contribute to voltage at node N5], based on the second resistance value, and

a switching stage [comparator 10] operably coupled to the first stage, the second stage, and the capacitor, and is configured to:

decrease a voltage on the capacitor when the voltage increases to the first voltage level, increase the voltage on the capacitor when the voltage decreases to the second voltage level,

wherein the first resistor substantially controls current flows, of substantially equal magnitude, through the first stage, the second stage, and the capacitor.

Regarding **claims 5 and 6**, Kodama discloses the oscillator of claim 4, wherein the second resistance value is selected based on the first resistance value, the first rate of change, the second rate of change (via feedback structure), and on a delay associated with a feedback loop of the oscillator (inherent propagation delays of comparator, inverter, etc.).

Regarding **claims 7 and 8**, Kodama discloses the oscillator of claim 5, but does not specifically disclose, "wherein a value of the second resistance value at a base temperature includes a factor of R.sub.d*(K1/(K2-K1)), and a value of the first resistance value at the base temperature is substantially equal to R.sub.d plus the value of the second resistance value at the base temperature, where R.sub.d corresponds to the difference between the first resistance value and the second resistance value at a base temperature, K1 is the first rate of change, and K2 is the second rate of change,

wherein the value of the second resistance value at the base temperature further includes a second factor of (D/C)*((Kd-K1)/(K2-K1)), where D is a delay associated with a feedback loop of the oscillator (200) at the base temperature, C is a capacitance value of the capacitor (C), and Kd is a rate of change of the delay with temperature."

All structural and functional limitations except the claimed equations of claims 7 and 8 appear to be met. Kodama's resistive regulation with respect to temperature tends to show evidence pointing towards the inherency of the claimed equations. Kodama appears to provide for resistive values of the first and second resistors dependent on delay of the feedback loop, capacitance of the capacitor 30, and delay with respect to temperature.

Additionally, as per MPEP section 2112:

V. ONCE A REFERENCE TEACHING PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS MADE THE BASIS OF A REJECTION, AND THE EXAMINER PRESENTS EVIDENCE OR REASONING

TENDING TO SHOW INHERENCY, THE BURDEN SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE

"[T]he PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his [or her] claimed product. Whether the rejection is based on inherency' under 35 U.S.C. 102, on prima facie obviousness' under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same...[footnote omitted]." The burden of proof is similar to that required with respect to product-by-process claims. In re Fitzgerald, 619 F.2d 67, 70, 205 USPQ 594, 596 (CCPA 1980) (quoting In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977)).

The applicant is thus invited to show an unobvious difference between the claimed invention of claims 7 and 8 and the device of Nolan in view of Kodama.

Regarding **claim 9**, Kodama discloses the oscillator of claim 1, wherein the first resistor is formed as a Ppoly resistor of a CMOS device, and the second resistor is formed as an Nwell resistor of the CMOS device (see lines 1-15 of column 4 and lines 12-28 of column 8 of Kodama).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Nolan et al. (US 6,356,161)*** in view of ***Kodama (US 6,300,843 - of record)***.

Regarding **claim 1**, line 48 of column 4 – line 40 of column 6 and Figs 3 and 4 of Nolan disclose an oscillator [1] comprising:

a first resistor [Rint 232], a second resistor [Rext 234], and a capacitor [C1, C2], wherein an oscillation frequency of the oscillator is dependent upon the resistance values for reducing variations in the oscillation frequency with temperature (see lines 25-40 of column 6).

Nolan suggests in lines 29-32 and 59-64 of column 6 using at least one resistor with a small linear temperature coefficient to regulate bias to amplifiers 220 and 320 of the CTAT and PTAT respectively, but does not specifically disclose, "wherein an oscillation frequency of the oscillator is dependent upon a difference between a first resistance value of the first resistor and a second resistance value of the second resistor, the first resistance value being larger than the second resistance value, the first resistor exhibits a first rate of change with temperature, and the second resistor exhibits a second rate of change with temperature that is larger than the first rate of change, thereby allowing temperature-induced changes to the first resistance value to be offset by changes to the second resistance value, and thereby reducing variations in the oscillation frequency with temperature."

However, Fig. 3 of Kodama discloses an oscillator [200] comprising:

a first resistor [121], a second resistor [123], and a capacitor [30], wherein an oscillation frequency of the oscillator is dependent upon a difference between a first

resistance value of the first resistor and a second resistance value of the second resistor, the first resistance value being larger than the second resistance value, the first resistor exhibits a first rate of change with temperature (regulation of resistance relative to temperature), and the second resistor exhibits a second rate of change with temperature that is larger than the first rate of change (see lines 12-14 of column 8), thereby allowing temperature-induced changes to the first resistance value to be offset by changes to the second resistance value, and thereby reducing variations in the oscillation frequency with temperature (see lines 57-67 of column 1).

The resistive ladders in figures 1 and 3 provide regulation to comparator 10 in order to stabilize oscillation frequency with respect to temperature.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a thermal resistive ladder structure, as disclosed by Kodama, into the CTAT and PTAT devices disclosed in Nolan for the purpose of further stabilizing oscillation frequency with respect to temperature.

Regarding **claims 2-4**, the device of Nolan in view of Kodama (with reference to Fig. 1 of Kodama) discloses the oscillator of claim 1, further comprising:

a first stage [resistances 21 and 23 and NMOS 29], operably coupled to the first resistor, that is configured to provide a first voltage level [at node N3 to contribute to voltage at node N5], based on the first resistance value,

a second stage [resistances 23 and 25 and NMOS 27], operably coupled to the second resistor, that is configured to provide a second voltage level [at node N4 to contribute to voltage at node N5], based on the second resistance value, and

a switching stage [comparator 10] operably coupled to the first stage, the second stage, and the capacitor, and is configured to:

decrease a voltage on the capacitor when the voltage increases to the first voltage level, increase the voltage on the capacitor when the voltage decreases to the second voltage level,

wherein the first resistor substantially controls current flows, of substantially equal magnitude, through the first stage, the second stage, and the capacitor.

Regarding **claims 5 and 6**, the device of Nolan in view of Kodama discloses the oscillator of claim 4, wherein the second resistance value is selected based on the first resistance value, the first rate of change, the second rate of change, and on a delay associated with a feedback loop of the oscillator.

Regarding **claims 7 and 8**, the device of Nolan in view of Kodama discloses the oscillator of claim 5, but does not specifically disclose, "wherein a value of the second resistance value at a base temperature includes a factor of R.sub.d*(K1/(K2-K1)), and a value of the first resistance value at the base temperature is substantially equal to R.sub.d plus the value of the second resistance value at the base temperature, where R.sub.d corresponds to the difference between the first resistance value and the second resistance value at a base temperature, K1 is the first rate of change, and K2 is the second rate of change,

wherein the value of the second resistance value at the base temperature further includes a second factor of (D/C)*((Kd-K1)/(K2-K1)), where D is a delay associated

with a feedback loop of the oscillator (200) at the base temperature, C is a capacitance value of the capacitor (C), and Kd is a rate of change of the delay with temperature."

All structural and functional limitations except the claimed equations of claims 7 and 8 appear to be met. Kodama's resistive regulation with respect to temperature tends to show evidence pointing towards the inherency of the claimed equations. The device of Nolan in view of Kodama appears to provide for resistive values of the first and second resistors dependent on delay of the feedback loop, capacitance of the capacitor 30, and delay with respect to temperature.

Additionally, as per MPEP section 2112:

V. ONCE A REFERENCE TEACHING PRODUCT APPEARING TO BE SUBSTANTIALLY IDENTICAL IS MADE THE BASIS OF A REJECTION, AND THE EXAMINER PRESENTS EVIDENCE OR REASONING TENDING TO SHOW INHERENCY, THE BURDEN SHIFTS TO THE APPLICANT TO SHOW AN UNOBVIOUS DIFFERENCE

"[T]he PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his [or her] claimed product. Whether the rejection is based on inherency' under 35 U.S.C. 102, on prima facie obviousness' under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same...[footnote omitted]." The burden of proof is similar to that required with respect to product-by-process claims. In re Fitzgerald, 619 F.2d 67, 70, 205 USPQ 594, 596 (CCPA 1980) (quoting In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977)).

The applicant is thus invited to show an unobvious difference between the claimed invention of claims 7 and 8 and the device of Nolan in view of Kodama.

Regarding **claim 9**, the device of Nolan in view of Kodama discloses the oscillator of claim 1, wherein the first resistor is formed as a Ppoly resistor of a CMOS device, and the second resistor is formed as an Nwell resistor of the CMOS device (see lines 1-15 of column 4 and lines 12-28 of column 8 of Kodama).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Applicant's Admitted Prior Art (APA)*** in view of ***Takenaka et al. (US 2002/0067215 – of record)***.

Regarding **claim 10**, Fig. 1 of APA discloses an oscillator (100) comprising:

a first stage (150a-R1-160a) that includes:

a diode-configured Pchannel device (150a) operably coupled to a first voltage source, a diode-configured Nchannel device (160a) operably coupled to a second voltage source, and a first resistor (R) operably coupled in series between the diode-configured P-channel (150a) and Nchannel (160a) devices, a first voltage level being provided at a first node [gate of 150a] that couples the first resistor (R1) to the diode-configured Pchannel device (150a); ;

a switching stage [110, 120, 130, 170] that is configured to control a voltage on a capacitor such that: the voltage is decreased when the voltage increases to the first voltage level, and the voltage is increased when the voltage decreases to the second

voltage level. The first and second voltage levels are provided for via the feedback from the capacitor C to the window comparator 110, 120.

APA does not specifically disclose, "a second stage that includes a Pchannel device operably coupled to the first voltage source and having a gate that is common to the first node, a diode-connected Nchannel device operably coupled to the second voltage source, and a second resistor operably coupled in series between the Pchannel device and the diode-configured Nchannel device of the second stage, a second voltage level being provided at a second node that couples the second resistor to the P-channel device."

However, Figs. 12C and 13A, paragraphs 120-125 and 131-137 of Takenaka discloses an amplitude control circuit [50] including a first branch [P41, R10, P40] and a second branch [N40, R11, N41] feeding a relaxation oscillator [5], the relaxation oscillator being similar to that of APA.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize dual resistive ladder structures (each structure similar to the first branch as disclosed by APA), as disclosed by Takenaka, into the RC oscillator of APA for the purpose of further stabilizing oscillation frequency and amplitude, for example, over process variations between N and P devices.

Claims 11-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Applicant's Admitted Prior Art (APA)*** in view of ***Takenaka et al. (US 2002/0067215 – of record)*** in further view of ***Kodama (US 6,300,843 - of record)***.

Regarding **claims 11-16**, the device of APA in view of Takenaka discloses the oscillator of claim 10, but does not disclose, "wherein the first resistor has a first temperature coefficient, and the second resistor has a second temperature coefficient that is substantially larger than the first temperature coefficient."

However, Fig. 3 of Kodama discloses an oscillator [200] comprising:

a first resistor [121], a second resistor [123], and a capacitor [30], wherein an oscillation frequency of the oscillator is dependent upon a difference between a first resistance value of the first resistor and a second resistance value of the second resistor, the first resistance value being larger than the second resistance value, the first resistor exhibits a first rate of change with temperature (regulation of resistance relative to temperature), and the second resistor exhibits a second rate of change with temperature that is larger than the first rate of change (see lines 12-14 of column 8), thereby allowing temperature-induced changes to the first resistance value to be offset by changes to the second resistance value, and thereby reducing variations in the oscillation frequency with temperature (see lines 57-67 of column 1).

The resistive ladders in figures 1 and 3 provide regulation to comparator 10 in order to stabilize oscillation frequency with respect to temperature.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a thermal resistive ladder structure, as disclosed by Kodama, into the first and second branches of APA in view of Takenaka, for the purpose of stabilizing oscillation frequency and amplitude with respect to temperature.

Regarding **claim 17**, the device of APA in view of Takenaka, in further view of Kodama (with reference to Kodama) discloses the oscillator of claim 10 (and as further discussed in claims 11-16), wherein the first resistor is formed as a Ppoly resistor of a CMOS device, and the second resistor is formed as an Nwell resistor of the CMOS device (see lines 1-15 of column 4 and lines 12-28 of column 8 of Kodama).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Guo (US 6,888,763) discloses a temperature and process compensated charge-pump oscillator, very relevant to the claimed invention. However, Guo is not prior art under 35 USC 102 or 103 due to lack of a prior filing or publication date.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James E. Goodley whose telephone number is (571)-272-8598. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JG

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